

# TSV KOZ separation 3DIC P&R area optimization methodology considering device impact by TSV

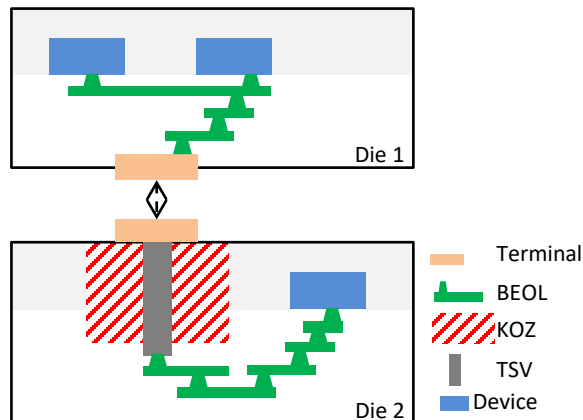
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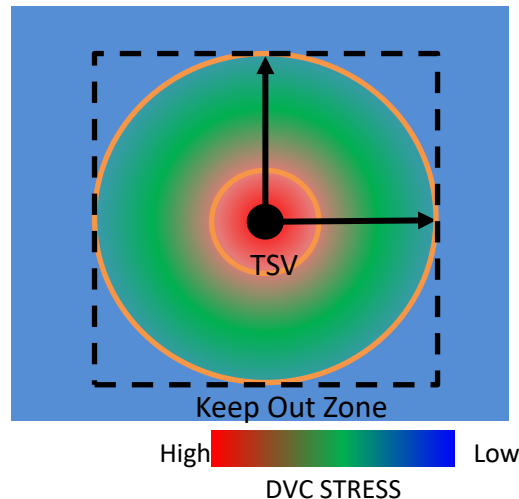


# Motivation

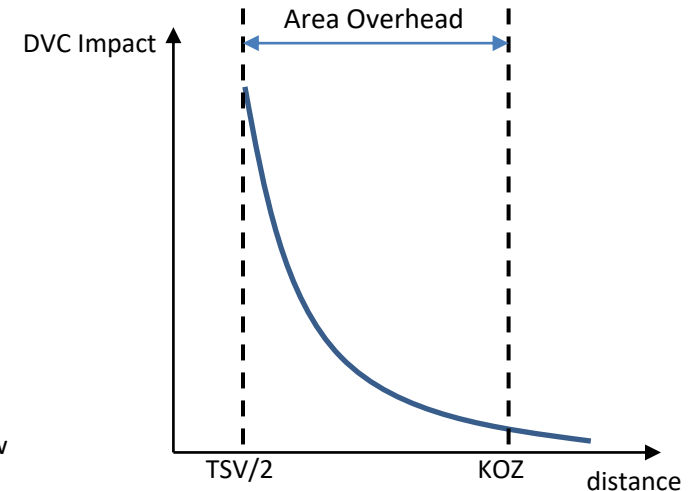
- For multi-die design, TSV (Through Silicon Via) is used to implement interconnection between dies
- 3DIC TSV Area Overhead
  - The TSV structure of several micrometers affects the surrounding devices.
  - Due to this stress, the device performance and reliability will vary within several micrometers of the TSV.
  - The extent of this stress increases as it gets closer to the TSV and has a significant impact on device performance.
  - The area where the DVC performance varies significantly due to stress is called the TSV Keep Out Zone (KOZ) and cannot be placed with logic devices."



<Multi die implementation example>



<Device Stress due to TSV process>

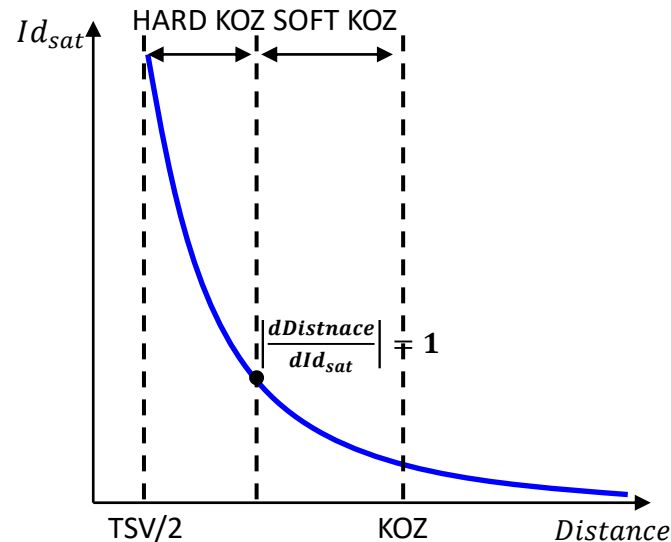
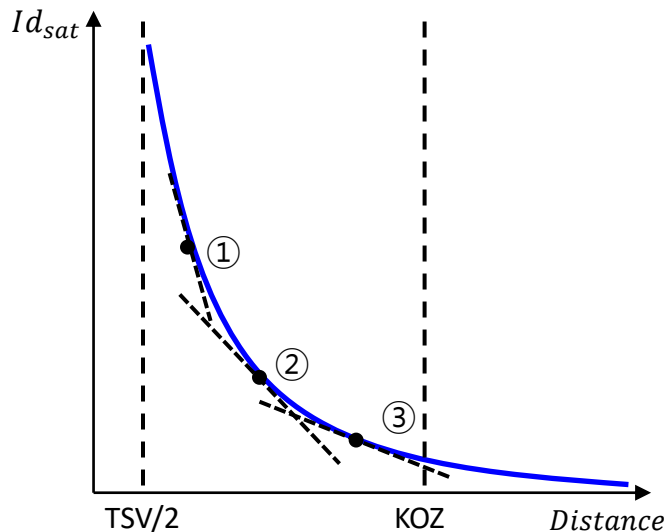


<Device Impact according to Distance>

# Main Idea

## Analysis of DVC Impact on TSV Stress

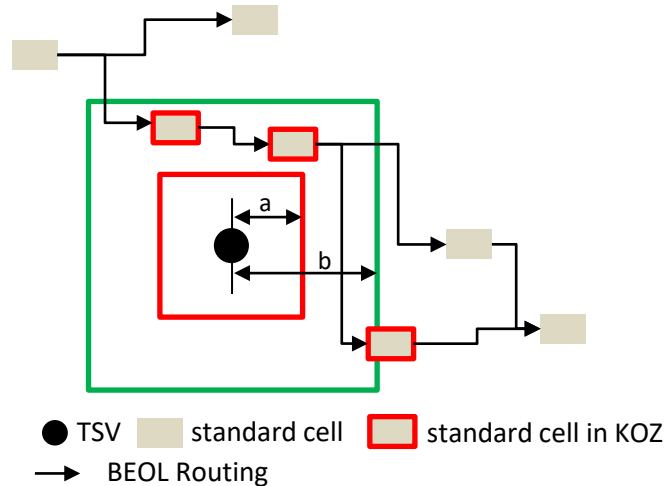
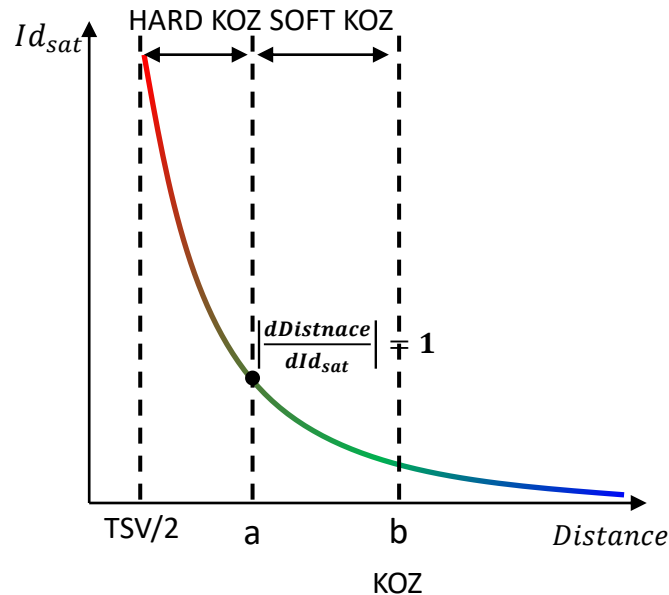
- TSV affect the saturation current( $I_{dsat}$ ) NMOS and PMOS of the device.
- We can interpret the variation of FET's  $I_{dsat}$  due to TSV by distance and divide it into Soft KOZ and Hard KOZ.
- The point where the magnitude of the change in FET's  $I_{dsat}$  according to the change in distance is less than 1 is defined as the Soft KOZ."
- On the graph point ① is a very large variation where  $\left| \frac{dDistance}{dI_{dsat}} \right| > 1$  point ② is a location where  $\left| \frac{dDistance}{dI_{dsat}} \right| = 1$  which separates Soft KOZ and Hard KOZ, and point ③ is a location that falls within Soft KOZ with  $\left| \frac{dDistance}{dI_{dsat}} \right| < 1$



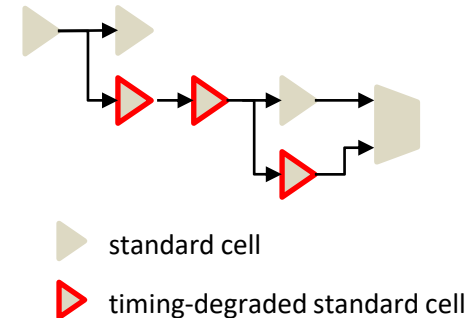
# Main Idea

## 🌐 The characteristics and usage of Soft and Hard KOZ in P&R and STA

- Since the impact of DVC performance is large in Hard KOZ, the placement of DVC and routing of metal are prohibited, except for dummy
- In Soft KOZ, since the impact of the TSV stress on the device can be predicted, the placement and routing of standard cells are allowed.
  - Specific IP or device placement can be excluded.
- The timing impact of cells within the KOZ is reflected in the timing analysis.
- Although there may be timing degradation, the area gain can be secured by reducing the TSV's KOZ.



Example of P&R using Soft KOZ

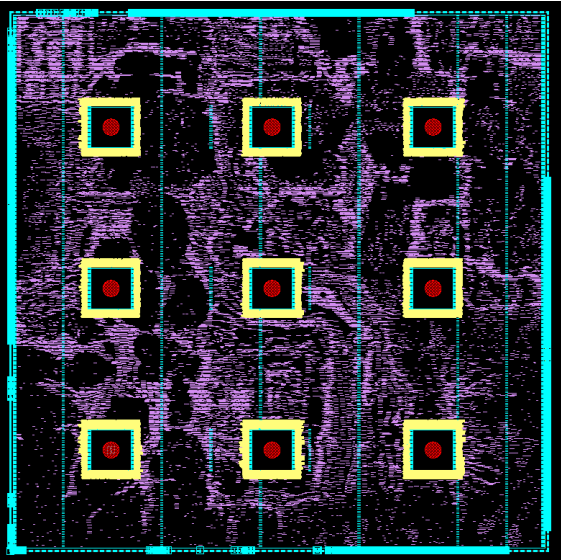


Example of STA using Soft KOZ

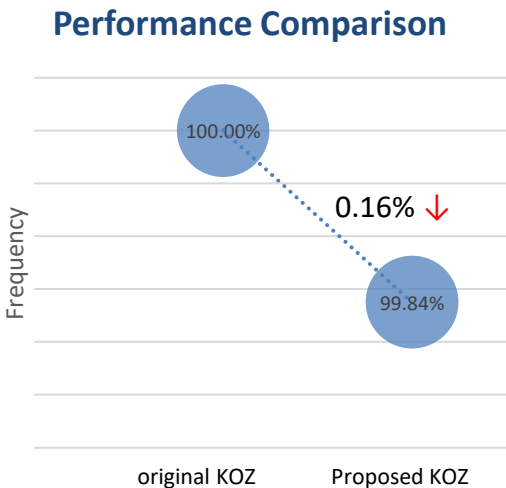
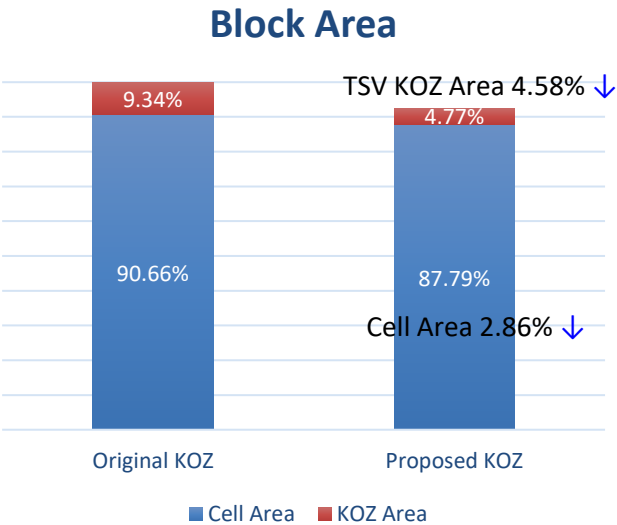
# Experimental Result

## PPA result in CPU Test Cases for the proposed TSV Keep Out Zone Structure

- We evenly placed 9 TSVs in the block (red circle), and the cells inside the Soft KOZ are highlighted in yellow.
- When the proposed KOZ method is applied, the area of the KOZ decreases by **4.58%** compared to the reference.
- In addition, the cell area also decreases by **2.86%**, resulting in a **7.44%** decrease in the overall block area.
- Due to the speed degradation of cells in the Soft KOZ, the speed of the top 300 critical paths at the block level is degraded by **0.16%**.



Block Layout



# Summary

- ⊗ TSVs affect surrounding devices, causing device performance and reliability to vary within several micrometers of the TSV.
- ⊗ TSVs affect the saturation current ( $I_{dsat}$ ) of NMOS and PMOS devices, which can be interpreted as the variation of FET's  $I_{dsat}$  with distance and divided into Soft KOZ and Hard KOZ.
- ⊗ In Hard KOZ, the placement of DVC and routing of metal are prohibited as the impact of DVC performance is large.
- ⊗ In Soft KOZ, the placement and routing of standard cells are allowed as the impact of TSV stress on the device can be predicted.
- ⊗ The timing impact of cells within the KOZ is reflected in the timing analysis.
- ⊗ When the proposed KOZ method is applied, the area of the KOZ decreases by 4.58% compared to the reference. The cell area decreases by 2.86%, resulting in a 7.44% decrease in the overall block area.
- ⊗ The speed of the top 300 critical paths at the block level is degraded by 0.16%.